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We, Koyo KATSURA, Shinichi KOJIMA and Noriyuki KURAKAMI, declare that:

We are subjects of Japan residing respectively at Hitachiota-shi, Maebashi-shi and Takasaki-shi, all of Japan;

We verily believe ourselves to be the original first and joint inventors of the invention described and claimed in the United States Letters Patent No. 4,975,857, and in the specification of the Reissue Application for which invention we solicit a Reissue patent;

We do not know and do not believe that said invention was ever known or used in the United States of America before our invention thereof;

We hereby state that we have reviewed and understand the contents of the specification of the Reissue Application, including the claims;

We acknowledge the duty to disclose information which is material to the examination of the Reissue Application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a);

We verily believe that the original patent to be wholly or partly inoperative or invalid by claiming less than we had a right to claim in the patent;

Specifically, during review of the specification and claims of U.S. Patent No. 4,975,857, subsequent to its issuance, undertaken as a result of discussions with another party concerning the technology of that party, it was found that the claims thereof were unduly limited in that they called for limitations not necessary to the patentable invention.

At meetings held in the United States of America on the dates of November 16 through November 20, 1992 with our U.S. Patent Attorneys, the claims of U.S. Patent No. 4,975,857 were studied in more detail and a new set of claims 9-43 were drafted at that time with the intention of presenting these claims in Reissue Application Serial No. 985,141.

Regarding the new claims 9-43, claim 9 is directed to a graphic processing apparatus including memory means for storing graphic data, data processing means for processing the graphic data, memory control means for controlling the transfer of graphic data to the data processing means, a first bus interconnecting the memory means and the memory control means to transfer M bits of data in parallel therebetween and a second bus interconnecting the data processing means and the memory control means to transfer in bits of data in parallel therebetween. In the graphic processing apparatus due to the difference in capacity between the first bus and the second bus a storage means is provided in the memory control means for temporarily storing graphic data sequentially read out via the first bus in a time

shared fashion form the memory means. The memory control means transfers the temporarily stored graphic data in parallel to the data processing means via the second bus.

Claim 10 is similar to claim 9 except that the memory control means includes multiplexing means for multiplexing graphic data received in parallel via the second bus from the data processing means. Also the memory control means of claim 10 transfers multiplexed graphic data sequentially in a time shared fashion to the memory means via the first bus.

Claim 11 recites a graphic processing apparatus including memory means having M bit terminals for storing graphic data wherein the graphic data is read out sequentially in a time shared fashion, and data processing means having N bit terminals for processing graphic data read from the memory means. N is greater than M. Interface means is provided having M bit terminals coupled to the memory means and N bit terminals coupled to the data processing means for transferring graphic data from the memory means to the data processing means. The interface means of the graphic processing apparatus of claim 11 includes converting means for converting sequential graphic data from the M bit terminals of the memory means into parallel graphic data to be supplied to the N bit terminals of the data processing means.

Claim 12 is similar to claim 11 except that the memory means has graphic data written sequentially thereto in a time shared fashion.

Claim 13 is similar to claim 9 except that the memory control means includes converting means for converting M bits of data sequentially read out in a time shared fashion from the memory means via the first bus into N bits of data to be supplied in parallel to the data processing means via the second bus and for converting N bits of data received in parallel from the data processing means via the second bus into M bits of data to be written sequentially to the memory means via the first bus in a time shared fashion.

Claim 14 depends from claim 13 and recites that the segmented M bits of data to be converted are sequentially read out of the memory means in a time shared fashion plural times within a predetermined unit of time based on an address specified by the data processing means.

Claim 15 depends from claim 14 and recites that the N bits of data converted from the M bits of data sequentially read out from the memory means is applied to the data processing means in a unit of time more than two times the predetermined unit of time.

Claim 16 depends from claim 13 and recites that the N bits of data each include an M bit portion of the N bits of data.

Claim 17 provides a data processing apparatus including data processing means for executing data processing, and memory means for storing data which is read out sequentially in a time shared fashion. Interface means is provided having M bit terminals coupled to the memory means and N bit terminals coupled to the data processing means.

The interface means controls the transfer of data between the memory means and the data processing means where N is greater than M. A bus having M lines interconnects the memory means and the interface means through the M bit terminals to transfer M bits of data in parallel therebetween. The interface means of the data processing apparatus of claim 17 includes converting means for converting sequential M bits of data from the memory means into N bits of parallel data to be supplied to the data processing means and for converting N bits of parallel data from the data processing means into sequential M bits of data to be written into the memory means.

Claim 18 depends from claim 17 and recites that the sequential M bits of data to be converted is sequentially read out of the memory means in a time shared fashion plural times within a predetermined unit of time based on the address specified by the data processing means.

Claim 19 depends from claim 18 and recites that the N bits of data converted from the M bits of data sequentially read out from the memory means is applied to the data processing means in a unit of time more than two times the predetermined unit of time.

Claim 20 depends from claim 17 and recites that the M bits of data includes an M bit portion of the N bits of data.

Claim 21 is directed to a memory read method for reading data from a memory in accordance with a request from a processor. The method includes the steps of reading out

M bits of data sequentially from the memory through an M bit bus in a time shared fashion for each of M bits based on an address specified by the processor where M is an integer, converting the read out M bits of data into N bits of parallel data where N is an integer and N is greater than M and applying the converted N bits of data to the processor through an N bit bus.

Claim 22 is similar to claim 21 except that claim 22 is directed to a memory write method for writing data generated in a processor in accordance with a request from the processor.

Claim 23 is directed to a memory controller for controlling transference of data between a memory and a processor where an M bit terminals are coupled to the memory, and N bit terminals are coupled to the processor. Converting means is provided between the N bit terminals and the M bit terminals for converting N bits of data into M bits of data. Claim 24 depends from claim 23 and recites that the M bits of data is sequentially read out of the memory in time shared fashion plural times within a predetermined unit of time. Claim 25 depends from claim 24 and recites that the N bits of data is applied to the processor in a unit of time more than two times the predetermined unit of time.

Claim 26 depends from claim 24 and recites that the M bits of data includes an M bit portion of the N bits of data. Claim 27 depends from claim 23 and recites that the converting means includes storage means for temporarily storing data.

Claim 28 is directed to a memory read method for reading data from a memory in accordance with a request from a processor wherein the data is read out from the memory sequentially in a time shared fashion plural times within a predetermined unit of time. The data read out is converted into parallel data and the parallel data is applied to the processor in a unit of time more than two times the predetermined unit of time. Claim 29 depends from claim 28 and recites that the sequentially read out data forms a portion of the parallel data to be applied to the processor. Claim 30 depends from claim 28 and recites that the data sequentially read out from the memory is composed of M bits of data and the parallel data is composed of N bits of data. Claim 31 depends from claim 30 and recites that N is equal to a predetermined number times M.

Claim 32 recites a method similar to claim 28 except that claim 32 recites a memory write method for writing data generated by a processor into a memory in accordance with a request from the processor. Claim 33 depends from claim 32 and recites that the data received in parallel from the processor is composed of N bits of data. Claim 34 which depends from claim 32 recites that the M bits of data includes an M bit portion of N bits of data.

Claim 35 is directed to a data processing apparatus which includes memory means, data processing means, and memory control means for controlling transfer of data between the memory means and the data processing means. A first bus is provided having M lines interconnecting the

memory means and the memory control means and a second bus having N lines interconnecting the data processing means and the memory control means wherein the memory control means includes converting means for converting M bits of data read out from the memory into N bits of data to be supplied in parallel to the data processing means. Claim 36 depends from claim 35 and recites that the M bits of data is succeessfully read out of the memory means in a time shared fashion plural times within a predetermined unit of time. Claim 37 depends from claim 36 and recites that the N bits of data converted from the M bits of data is applied to the data processing means in a unit of time more than two times the predetermined unit of time. Claim 38 depends from claim 35 and recites that the N bits of data includes M bit portions of the N bits of data. Claim 39 depends from claim 36 and recites that the M bits of data includes an N bit portion of N bits of data.

Claim 40 recites a memory control apparatus having interface means having M bit terminals coupled to a memory and N bit terminals coupled to data processing means. The interface means converts M bits of data from the memory means into N bits of data to be supplied to the data processing means. Claim 41 depends from claim 40 and recites that the M bits of data includes an M bit portion of N bits of data.

Claim 42 is similar to claim 28 but recites that the converting step is performed by converting the successively read out data into parallel data by combining the successively read out data.

Claim 43 is directed to a memory controller for controlling transference of data between a memory and a processor similar to claim 40 except that claim 43 recites that M bit terminals are coupled to the memory, and N bit terminals are coupled to the processor. Converting means is provided for converting M bits of data into M bits of parallel data.

The above-enumerated deficiencies in the original patent arose without any deceptive intention on our part. More particularly, the errors arose during the prosecution of U.S. Application Serial No. 302,332 filed January 27, 1989 from which U.S. Patent 4,975,857 due to our failure and that of our Japanese agent and U.S. attorneys to recognize that the specification originally presented and amended by the Amendments filed on April 5, 1990 and September 10, 1990, did not clearly describe Applicants' invention as it relates to the conventional system as a result of having failed to fully and appropriate appreciate the full extent of Applicants' invention;

We hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Japanese Patent Application No. 63-93448, filed April 18, 1988, in Japan.

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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CONSENT OF ASSIGNEE

The undersigned assignee of the entire interest in the above-mentioned Letters Patent No. 4,975,857 hereby assent to the accompanying application.

HITACHI, LTD.

1993-4-16
Date

Katsuo Ogawa
Katsuo OGAWA, Patent Attorney
General Manager, Patent Dept.

9. A graphic processing apparatus comprising:

memory means for storing graphic data:

data processing means for executing a predetermined processing on graphic data read out from the memory means;

memory control means for controlling transference of graphic data stored in said memory means to said data processing means in accordance with a request from said data processing means;

a first bus having m lines and interconnecting said memory means and said memory control means to transfer m bits of data in parallel therebetween, where m is an integer; and

a second bus having n lines and interconnecting said data processing means and said memory control means to transfer n bits of data in parallel therebetween, where n is an integer and n>m;

wherein said memory control means includes storage means for temporarily storing graphic data sequentially read out via said first bus in a time shared fashion from said memory means, said memory control means transfers the temporarily stored graphic data in parallel to said data processing means via said second bus.

10. A graphic processing apparatus comprising:

memory means for storing graphic data;

data processing means for executing a predetermined processing to generate graphic data;

memory control means for controlling transference of graphic data generated by said data processing means to said memory means in accordance with a request from said data processing means;

a first bus having m lines and interconnecting said memory means and said memory control means to transfer m bits of data in parallel therebetween, where m is an integer; and

a second bus having n lines and interconnecting said data processing means and said memory control means to transfer n bits of data in parallel therebetween, where n is an integer and n>m;

wherein said memory control means includes multiplexing means for multiplexing graphic data received in parallel via said second bus from said data processing means, said memory control means transfers multiplexed graphic data sequentially in a time shared fashion to said memory means via said first bus.

11. A graphic processing apparatus comprising:

memory means, having m bit terminals, for storing graphic data, said graphic data being read out sequentially from the memory means in a time shared fashion, where m is an integer;

data processing means, having n bit terminals, for executing a predetermined processing on graphic data read out from said memory means, said graphic data being supplied to said data processing means in parallel, where n is an integer and n>m;

interface means, having m bit terminals coupled to said memory means and n bit terminals coupled to said data processing means, for transferring graphic data stored in said memory means to said data processing means in accordance with a request from said data processing means;

wherein said interface means includes converting means for converting sequential graphic data read out from said memory means into parallel graphic data to be supplied to said data processing means.

12. A graphic processing apparatus comprising:

memory means, having m bit terminals, for storing graphic data, said graphic data being written sequentially into said memory means in a time shared fashion, where m is an integer;

data processing means, having n bit terminals, for executing a predetermined processing to generate graphic data, said generated graphic data being transferred as parallel data, where n is an integer and n>m;

interface means, having m bit terminals coupled to said memory means and n bit terminals coupled to said data processing means, for transferring graphic data generated by said data processing means to said memory means in accordance with a request from said data processing means;

wherein said interface means includes converting means for converting parallel graphic data from said data processing means into sequential graphic data to be supplied to said memory means.

[13. A data processing apparatus comprising:

memory means for storing data;

data processing means for executing a predetermined data processing;

memory control means for controlling transference of data between said memory means and said data processing means in accordance with a request from said data processing means;

a first bus having m lines and interconnecting said memory means and said memory control means to transfer m bits of data in parallel therebetween, where m is an integer; and

a second bus having n lines and interconnecting said data processing means and said memory control means to transfer n bits of data in parallel therebetween, where n is an integer and n>m;

wherein said memory control means includes converting means for converting m bits of data sequentially read out in a time shared fashion from said memory means via said first bus into n bits of data to be supplied in parallel to said data processing means via said second bus and for converting n bits of data received in parallel from said data processing means via said second bus into m bits of data to be written sequentially to said memory means via said first bus in a time shared fashion.]

A 14. A graphic ~~data~~ processing apparatus according to claim 9, ~~13~~ wherein said segmented m bits of data to be converted are sequentially read out of said memory means in a time shared

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fashion plural times within a predetermined unit of time based on an address specified by said data processing means.

[15. A data processing apparatus according to claim 14 wherein said n bits of data converted from said m bits of data sequentially read out from said memory means is applied to said data processing means in a unit of time more than two times said predetermined unit of time.]

16. A data processing apparatus according to claim ~~13~~ 9 wherein said m bits of data each include an m bit portion of said n bits of data.

[17. A data processing apparatus comprising:

data processing means for executing a predetermined data processing;

memory means for storing data, wherein said data is read out sequentially from said memory means in a time shared fashion;

interface means, having m bit terminals coupled to said memory means and n bit terminals coupled to said data processing means, for controlling transference of data between said memory means and said data processing means in accordance with a request from said data processing means, where m and n are both integers and n>m;

a bus having m lines and interconnecting said memory means and said interface means through said m bit terminals to transfer m bits of data in parallel therebetween;

wherein said interface means includes converting means for

converting sequential m bits of data from said memory means into n bits of parallel data to be supplied to said data processing means and for converting n bits of parallel data from said data processing means into sequential m bits of data to be written into said memory means.]

18. A data processing apparatus according to claim ~~17~~ 11 wherein said sequential m bits of data to be converted is sequentially read out of said memory means in a time shared fashion plural times within a predetermined unit of time based on an address of specified by said data processing means.

19. A data processing apparatus according to claim ~~18~~ 11 wherein said n bits of data converted from said m bits of data sequentially read out from said memory means is applied to said data processing means in a unit of time more than two times said predetermined unit of time.

20. A data processing apparatus according to claim ~~17~~ 11 wherein said m bits of data each includes an m bit portion of said n bits of data.

21. A memory read method for reading data from a memory in accordance with a request from a processor, comprising the steps of:

reading out m bits of data sequentially from said memory through an m-bit bus in a time shared fashion for each m bits based on an address specified by said processor, where m is an

integer;

converting said read out m bits of data into n bits of parallel data, where n is an integer and n>m; and

applying said converted n bits of data to said processor through an n-bit bus.

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22. A memory write method for writing data generated in a processor into a memory in accordance with a request from said processor, comprising the steps of:

receiving n bits of data in parallel from said processor through an n-bit bus, where n is an integer;

converting said received n bits of parallel data into m bits of data, where m is an integer and n>m; and

writing said converted m bits of data sequentially into said memory through an m-bit bus in a time shared fashion based on an address specified by said processor.

23. A memory controller for controlling transference of data between a memory and a processor, said memory controller comprising:

m bit terminals for coupling to said memory, wherein m bits of data is transferred sequentially through said m bit terminals between said memory and said controller in a time shared fashion, where m is an integer;

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit

terminals between said controller and said processor, where n is an integer and n>m; and

converting means for making a conversion between n bits of data from said n bit terminals and a plurality of m bits of data from said m bit terminals corresponding thereto.

24. A memory controller according to claim 23 wherein said m bits of data from said m bit terminals to be converted is sequentially read out of said memory in a time shared fashion plural times within a predetermined unit of time based on an address specified by said processor.

25. A memory controller according to claim 24 wherein said n bits of data from said n bit terminals to be converted is applied to said processor in a unit of time more than two times said predetermined unit of time.

26. A memory controller according to claim 23 wherein said m bits of data each includes an m bit portion of said n bits of data.

27. A memory controller as claimed in claim 23, wherein said converting means includes storage means for temporarily storing data.

28. A memory read method for reading data from a memory in accordance with a request from a processor, comprising the steps of:

reading out data sequentially from said memory in a time shared fashion plural times within a predetermined unit of time based on an address specified by said processor;

converting said read out data into parallel data; and

applying said converted data to said processor in a unit of time more than two times said predetermined unit of time.

29. A memory read method according to claim 28 wherein each of said data sequentially read out from said memory forms a portion of said parallel data to be applied to said processor.

30. A memory read method according to claim 28 wherein said data sequentially read out from said memory is composed of m bits of data, said parallel data applied to said memory is composed of n bits of data and wherein both n and m are integers and n>m.

31. A memory read method according to claim 30 wherein n is equal to a predetermined number times m.

32. A memory write method for writing data generated by a processor into a memory in accordance with a request from said processor, comprising the steps of:

receiving data in parallel from said processor within a predetermined unit of time;

converting said received parallel data into sequential data each having a portion of said received parallel data; and

writing said converted data sequentially into said memory based on an address specified by said processor in a time shared fashion plural times in a unit of time less than one half said predetermined unit of time.

33. A memory write method according to claim 32 wherein said data received in parallel from said processor is composed of n bits of data and said converted data to be sequentially written into said memory is composed of m bits of data where m and n are both integers and n>m.

34. A memory write method according to claim 32 wherein said m bits of data each includes an m bit portion of said n bits of data.

35. A data processing apparatus comprising:

memory means for storing data;

data processing means for executing a predetermined data processing;

memory control means for controlling transfer of data between said memory means and said data processing means in accordance with a request from said data processing means;

a first bus having m lines and interconnecting said memory means and said memory control means to transfer m bits of data in parallel therebetween, where m is an integer; and

a second bus having n lines and interconnecting said data processing means and said memory control means to transfer n

bits of data in parallel therebetween, where n is an integer and n>m;

wherein said memory control means includes converting means for converting m bits of data successively read out from said memory means via said first bus into n bits of data to be supplied in parallel to said data processing means via said second bus and for converting n bits of data received in parallel from said data processing means via said second bus into m bits of data to be successively written to said memory means via said first bus.

36. A data processing apparatus according to claim 35 wherein said m bits of data to be converted is successively read out of said memory means in a time shared fashion plural times within a predetermined unit of time based on an address specified by said data processing means.

37. A data processing apparatus according to claim 36 wherein said n bits of data converted from said m bits of data successively read out of said memory means is applied to said data processing means in a unit of time more than two times said predetermined unit of time.

38. A data processing apparatus according to claim 35 wherein said m bits of data each includes an m bit portion of said n bits of data.

39. A memory control apparatus according to claim 36 wherein said m bits of data each includes an m bit portion of said n bits of data.

40. A memory control apparatus for controlling a memory of data processing means, said memory control apparatus comprising:

interface means, having m bit terminals to be coupled to said memory and n bit terminals to be coupled to said data processing means, for controlling transference of data between said memory and said data processing means in accordance with a request from said data processing means, where m and n are both integers and n>m;

wherein said interface means includes converting means for converting successive m bits of data from said memory means into n bits of data to be supplied to said data processing means and for converting n bits of data from said data processing means into successive m bits of data to be written into said memory.

41. A memory controller according to claim 40 wherein said m bits of data each includes an m bit portion of said n bits of data.

42. A memory read method for reading data from a memory in accordance with a request from a processor, comprising the steps of:

reading out data successively from said memory in a time shared fashion plural times within a predetermined unit of time based on an address specified by said processor;

converting said successively read out data into parallel data by combining said successively read out data; and

applying said converted data to said processor in a unit of time more than two times said predetermined unit of time.

43. A memory controller for controlling transference of data between a memory and a processor, said memory controller comprising:

m bit terminals for coupling to said memory, wherein a predetermined number of m bits of parallel data is transferred successively in a predetermined unit of time through said m bit terminals between said memory and said controller, where m is an integer;

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit terminals between said controller and said processor where n is an integer, n>m and said predetermined number times m equals n; and

converting means for making a conversion between n bits of data from said n bit terminals and said predetermined number of successive m bits of parallel data from said m bit terminals.

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